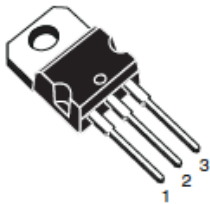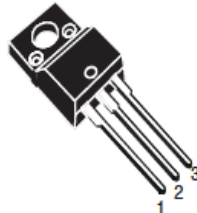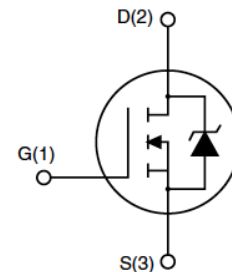## Description

650V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

Features

- $R_{DS(ON)} = 1.27\Omega$ (Max.) @ $V_{GS} = 10V$, $I_D = 3.5A$
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

Application

- DC-DC & DC-AC Converters
- Uninterruptible Power Supply (UPS)
- Switch Mode Low Power Supplies

Package

TO-220

TO-220F

Absolute Maximum Ratings $T_C=25℃$ unless otherwise specified

Symbol	Parameter		Max.		Units
			TO-220	TO-220F	
V_{DSS}	Drain-Source Voltage		650		V
V_{GSS}	Gate-Source Voltage		± 30		V
I_D	Continuous Drain Current	$T_C = 25℃$	7	7*	A
		$T_C = 100℃$	4.3	4.3*	A
I_{DM}	Pulsed Drain Current note1		28	28*	A
E_{AS}	Single Pulsed Avalanche Energy note2		200		mJ
dv/dt	Peak Diode Recovery Energy note3		4.5		V/ns
P_D	Power Dissipation	$T_C = 25℃$	125	30	W
	Linear Derating Factor	$T_C > 25℃$	1	0.24	W/℃
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1	4.2	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		62.5	62.5	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		℃

*Drain current limited by maximum junction temperature

Electrical Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250mA	650	-	-	V
$\triangle V_{(BR)DSS}$ /$\triangle T_J$	Breakdown Voltage Temperature Coefficient	Reference to 25℃, I_D = 250μA	-	0.5	-	V/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 520V, T_C = 125℃	-	-	50	μA
I_{GSS}	Gate to Body Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-	-	±10	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage [note4]	V_{DS} = V_{GS}, I_D = 250μA	2	-	4	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} =10V, I_D = 3.5A	-	1.0	1.27	Ω
g_{FS}	Forward Transconductance	V_{DS} =15V, I_D = 3.5A	-	6	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	-	1145	-	pF
C_{oss}	Output Capacitance		-	130	-	pF
C_{rss}	Reverse Transfer Capacitance		-	28	-	pF
Q_g	Total Gate Charge	V_{DD} = 520V, I_D = 7A, V_{GS} = 10V	-	41	-	nC
Q_{gs}	Gate-Source Charge		-	7.5	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	22	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 325V, I_D = 3.5A, R_G = 4.7Ω, V_{GS} = 10V	-	20	-	ns
t_r	Turn-On Rise Time		-	12	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	45	-	ns
t_f	Turn-Off Fall Time		-	15	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	7	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	28	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_S = 7A	-	-	1.6	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_F = 7A, di/dt =100A/μs	-	400	-	ns
Q_{rr}	Reverse Recovery Charge		-	2.6	-	uC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. L = 10mH, I_{AS} = 7A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C

3. I_{SD} ≤ 7A, di/dt ≤ 200A/μs, V_{DD} ≤ B_{VDSS}, Starting T_J = 25°C

4. Pulse width ≤ 300μs; duty cycle ≤ 2%.

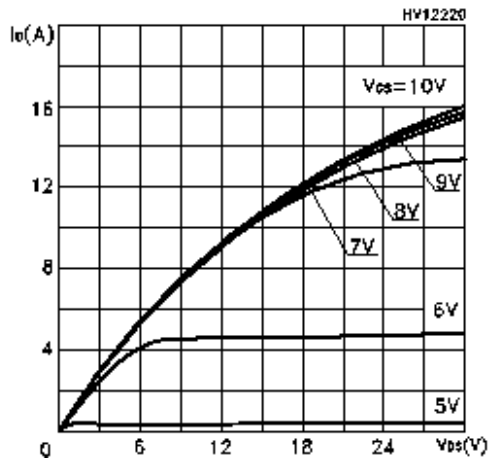# Typical Performance Characteristics
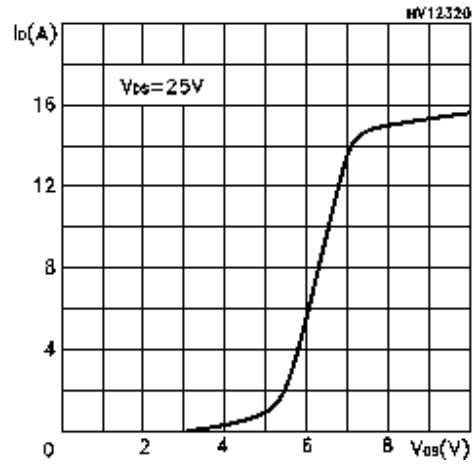
Figure 1. Output Characteristics
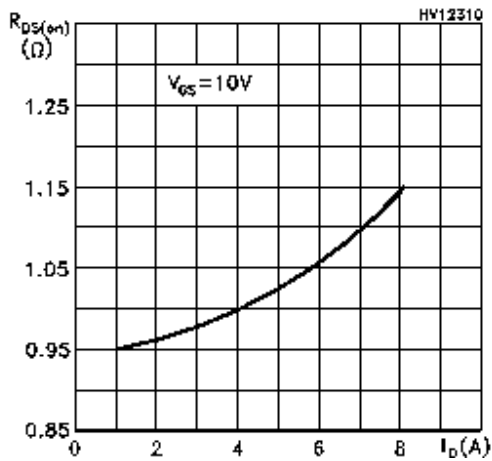
Figure 2. Transfer Characteristics

Figure 3. Drain-to-Source On Resistance vs.
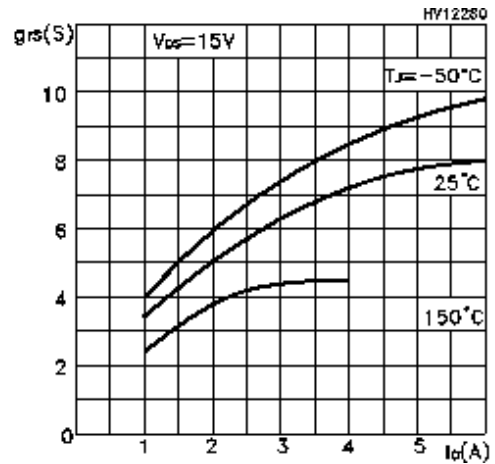Drain Current and Gate Voltage

Figure 4. Body Diode Forward Voltage vs.
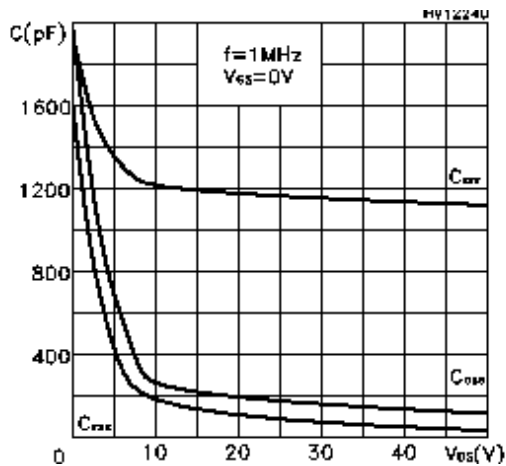Source Current and Temperature
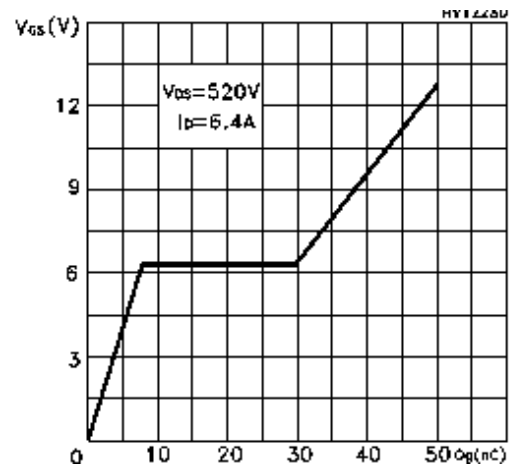
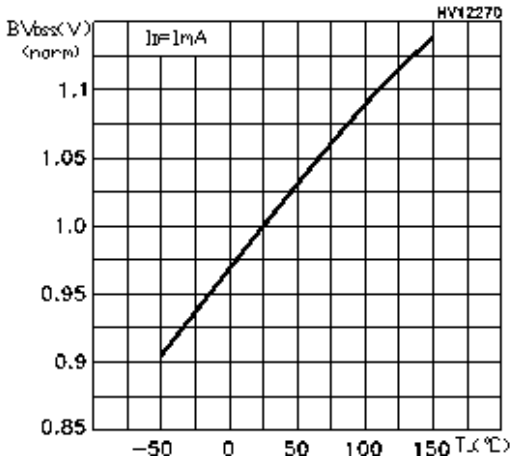Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

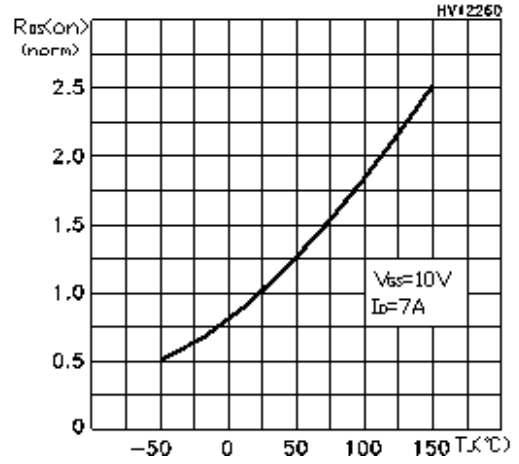Figure 7. Normalized Breakdown Voltage vs. Junction Temperature

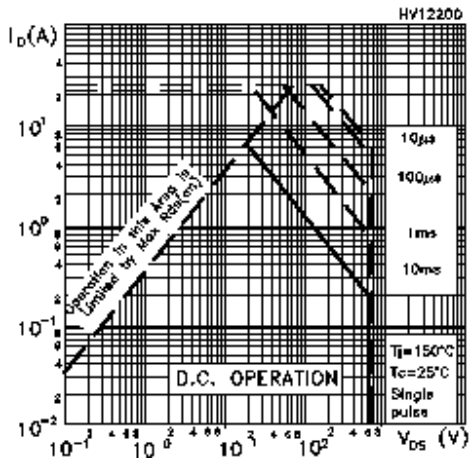Figure 8. Normalized On Resistance vs. Junction Temperature
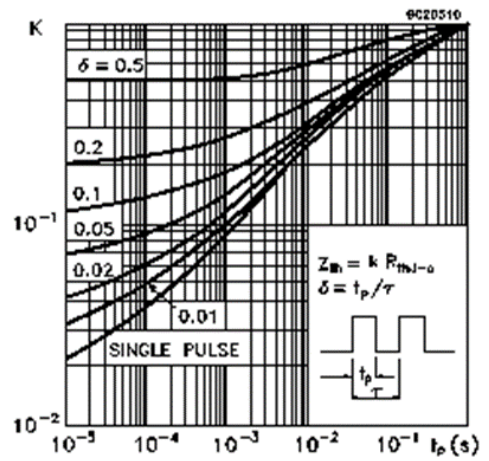
Figure 9. Maximum Safe Operating Area

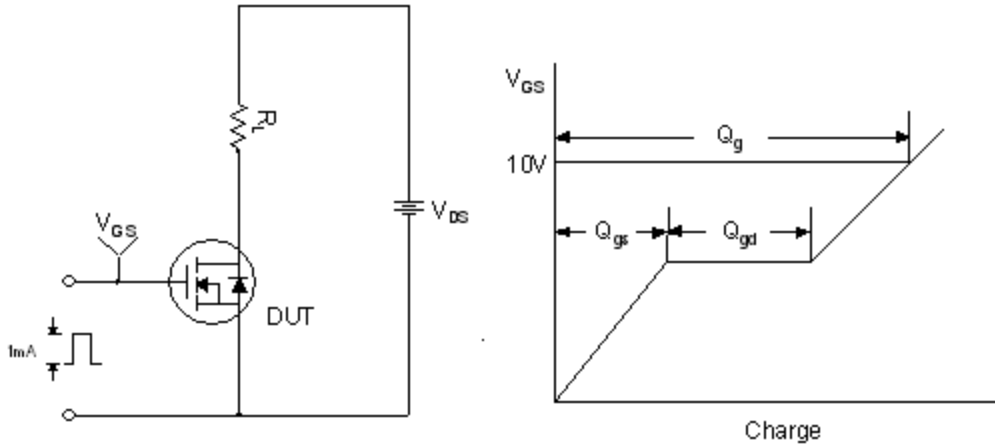Figure 10. Maximum Effective Transient Thermal Impedance, Junction-to-Case

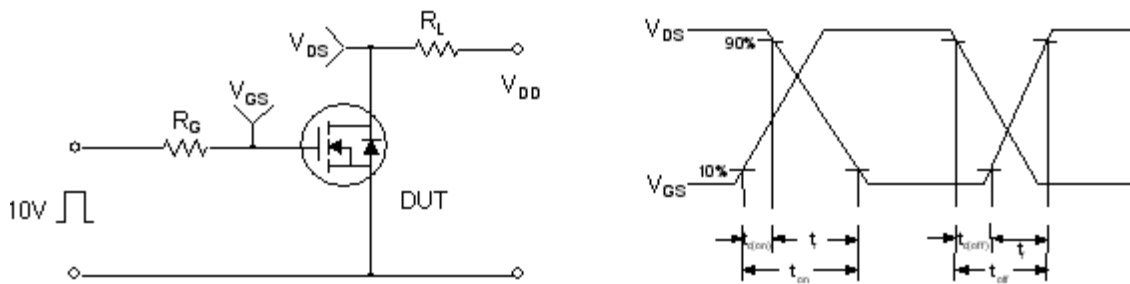**Figure 11. Gate Charge Test Circuit & Waveform**

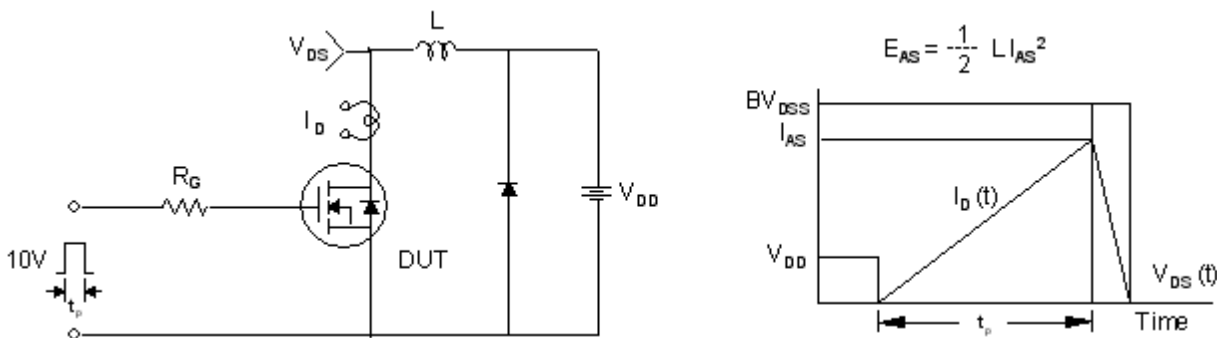**Figure 12. Resistive Switching Test Circuit & Waveforms**

$$E_{AS} = \frac{1}{2} L I_{AS}^2$$

Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms

D.U.T

Circuit Layout Considerations
* Low Stray Inductance
* Ground Plane
* Low Leakage Inductance Current Transformer

③

②

④

①

R_G

* dv/dt controlled by R_G
* Driver same type as D.U.T.
* I_{SD} controlled by Duty Factor "D"
* D.U.T. - Device Under Test

V_{DD}

① Driver Gate Drive

P.W. — Period

$D = \dfrac{P.W.}{Period}$

$V_{GS}=10V$ *

② D.U.T. I_{SD} Waveform

Reverse Recovery Current

Body Diode Forward Current

di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery dv/dt

V_{DD}

Re-Applied Voltage

Body Diode Forward Drop

④ Inductor Curent

Ripple ≤ 5%

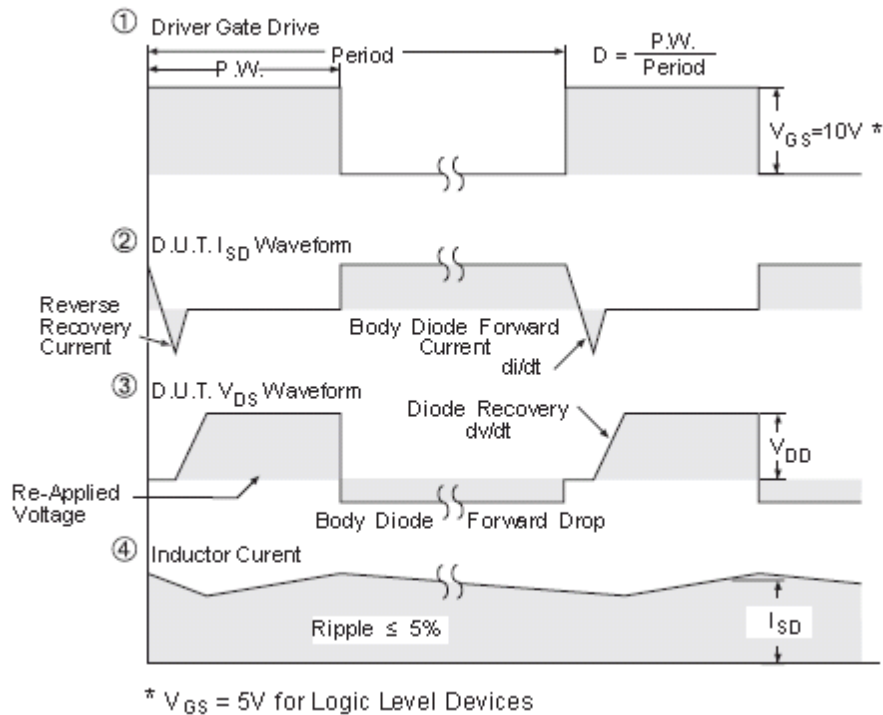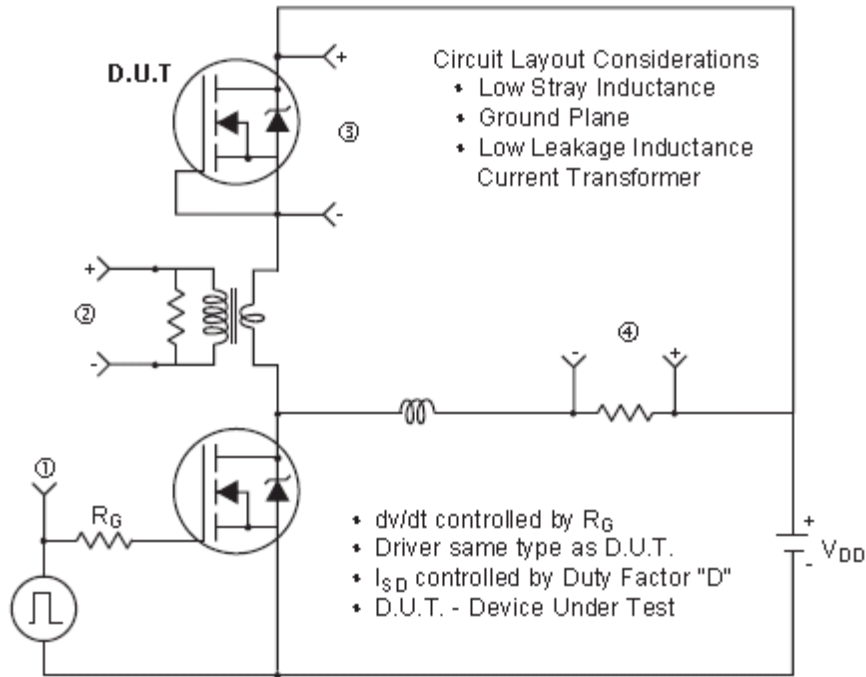I_{SD}

* V_{GS} = 5V for Logic Level Devices

Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)