

18V Output 800KHz Boost Regulator

Features

- 2.1V to 5.5V Input Voltage
- Up to 18V Output Voltage
- Integrated 60mΩ Power MOSFET
- 800KHz Fixed Switching Frequency
- Internal 4A Switch Current Limit
- Internal Compensation
- Thermal Shutdown
- Output Adjustable from 0.6V
- -40°C to +85°C Temperature Range
- Available in a SOT23-6 package

Applications

- Digital Set-top Box (STB)
- Tablet Personal Computer (Pad)
- LCD Bias Supply
- Battery-Powered Equipment
- Portable Media Player (PMP)
- General Purposes

General Description

The TX9715 is a constant frequency, current mode step-up converter intended for small, low power applications. The TX9715 switches at 800KHz and allows the use of tiny, low cost capacitors and inductors 2mm or less in height. Internal soft-start results in small

inrush current and extends battery life.

The TX9715 includes under-voltage lockout, current limiting, and thermal overload protection to prevent damage in the event of an output overload. The TX9715 is available in a small SOT23-6 package.

Typical Application

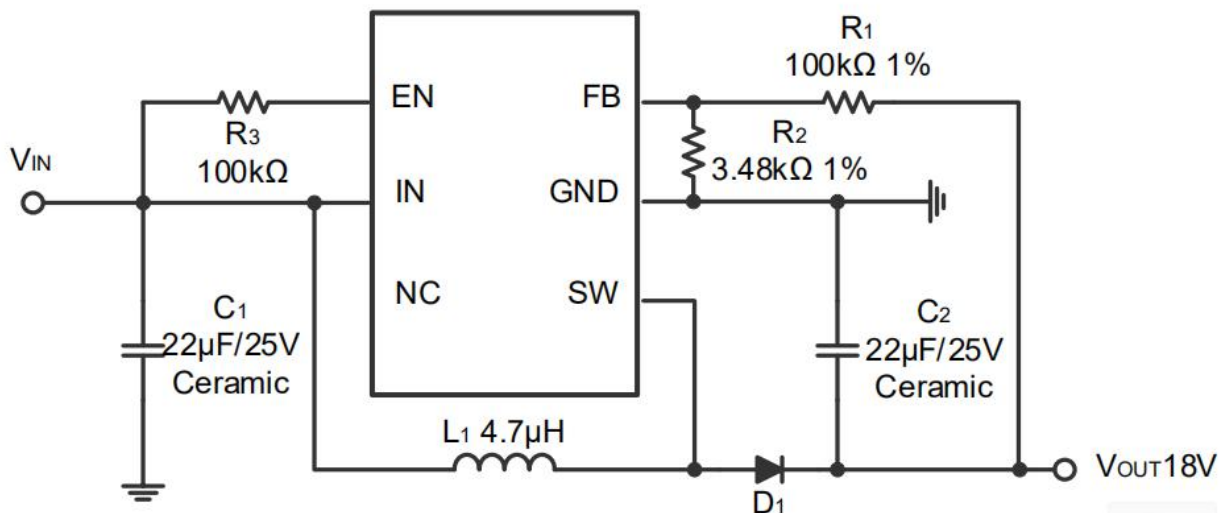


Figure1. Basic Application Circuit

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Functional Block Diagram

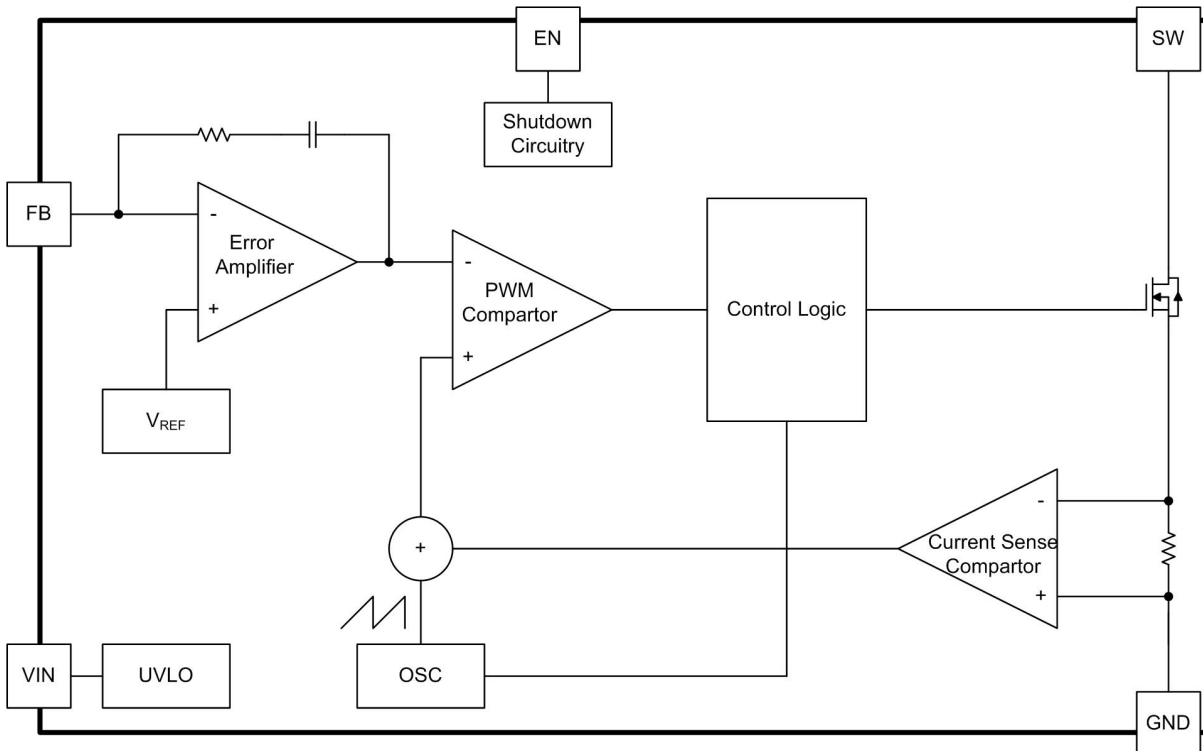


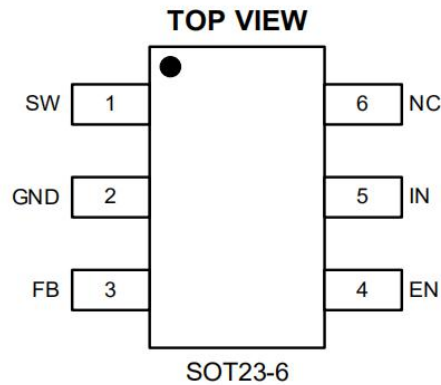
Figure 1. TX9715 Block Diagram

Pin Description

Pin	Name	Function
1	SW	Power Switch Output. SW is the drain of the internal MOSFET switch. Connect the power inductor and output rectifier to SW.
2	GND	Ground Pin
3	FB	Feedback Input. The FB voltage is 0.6V. Connect a resistor divider to FB.
4	EN	Regulator On/Off Control Input. A high input at EN turns on the converter, and a low input turns it off. When not used, connect EN to the input supply for automatic startup.
5	IN	Input Supply Pin. Must be locally bypassed.
6	NC	Not Connection

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Package/order Information



Top Marking: KHYLL (device code: KH, Y=year code, LL= lot number code)

Marking	Part No.	Model	Description	Package	MOQ
KHYLL	70390013	TX9715	TX9715 Boost, VIN 2.1-5.5V, VOUT VIN- 18V, 800kHz, VFB 0.6V, SOT23-6	SOT23-6	3000PCS

Note : All TXCHIP parts are Pb-Free and adhere to the RoHS directive.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

Item	Min	Max	Unit
VIN EN voltage	-0.3	6	V
SW voltage	-0.3	20	V
All Other Pins	-0.3	6	V
Power dissipation ⁽³⁾	Internally Limited		
Operating junction temperature, T _J	-40	150	°C
Storage temperature, T _{stg}	-65	150	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, R_{θJA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: PD (MAX) = (T_J(MAX) – T_A)/R_{θJA}. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160°C (typical) and disengages at T_J= 130°C (typical).

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ESD Ratings

Item	Description	Value	Unit
$V_{(ESD-HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	± 2000	V
$V_{(ESD-CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	± 200	V
$I_{LATCH-UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	± 150	mA

Recommended Operating Conditions

Item	Min	Max	Unit
Operating junction temperature ⁽¹⁾	-40	125	°C
Operating temperature range	-40	85	°C
Input voltage VIN	2.1	5.5	V

Note (1): All limits specified at room temperature ($T_A = 25^{\circ}\text{C}$) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Thermal Information

Item	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾	105	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.5	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board.

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Electrical Characteristics ⁽¹⁾⁽²⁾

Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Current(Shutdown)	$V_{EN}=0V$		0.1	1	μA
Quiescent Current (PFM)	$V_{FB}=0.7V$, No switch		50	100	μA
Quiescent Current (PWM)	$V_{FB}=0.5V$, switch		0.2	0.4	mA
SW Leakage	$V_{SW} = 20V$			1	μA
SW On Resistance			60	120	m Ω
Operating Input Voltage		2.1		5.5	V
Current Limit	$V_{IN}= 5V$,Duty cycle=50%		4		A
Oscillator Frequency			800		KHz
Maximum Duty Cycle	$V_{FB}=0.5V$		90		%
Feedback Voltage		588	600	612	mV
FB Input Bias Current	$V_{FB}=0.6V$	-50	-10		nA
EN Rising Threshold		1.2			V
EN Falling Threshold				0.8	V
EN Threshold Hysteresis			100		mV
Under-Voltage Lockout Threshold	Wake up V_{IN} Voltage		2.0	2.1	
	Shutdown V_{IN} Voltage	1.7	1.8	V	
Thermal Shutdown				160	$^{\circ}C$

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

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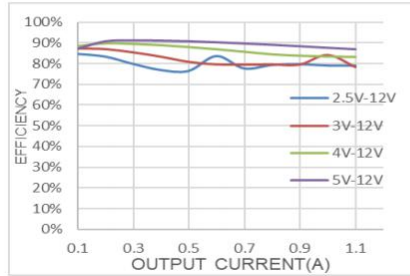
Typical Performance Characteristics (1) (2)

Note (1): Performance waveforms are tested on the evaluation board.

Note (2): $V_{IN} = 5V$, $V_{OUT} = 12V$, $T_A = +25^{\circ}C$, unless otherwise noted.

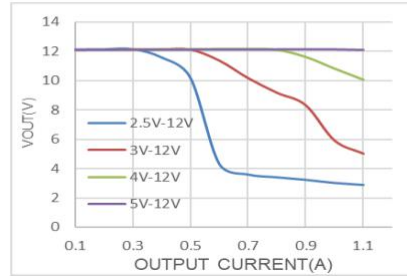
Efficiency vs. Load Current

$V_{out} = 12V$



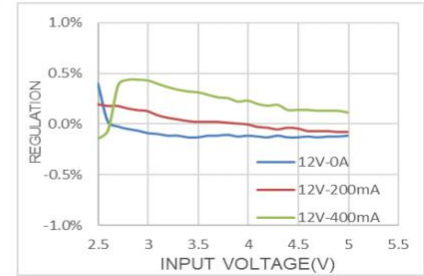
Load Regulation

$V_{out} = 12V$



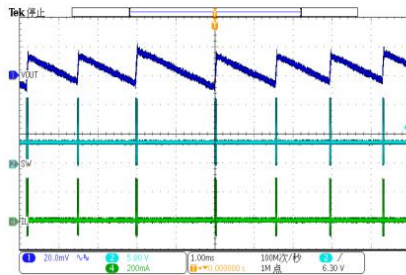
Line Regulation

$V_{out} = 12V$



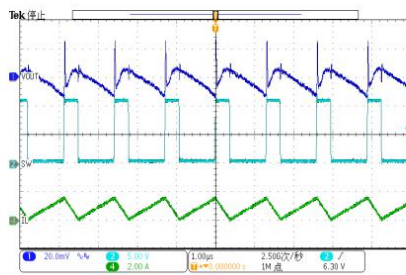
Output Ripple Voltage

$V_{IN} = 5V$, $V_{OUT} = 12V$, $I_{OUT} = 0A$



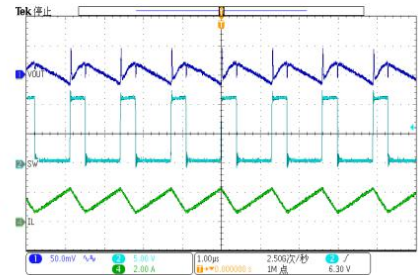
Output Ripple Voltage

$V_{IN} = 5V$, $V_{OUT} = 12V$, $I_{OUT} = 200mA$



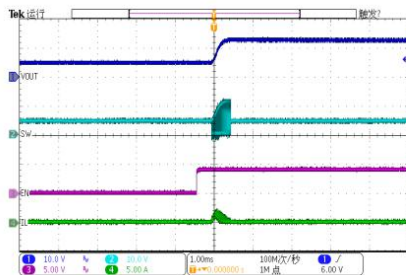
Output Ripple Voltage

$V_{IN} = 5V$, $V_{OUT} = 12V$, $I_{OUT} = 400mA$



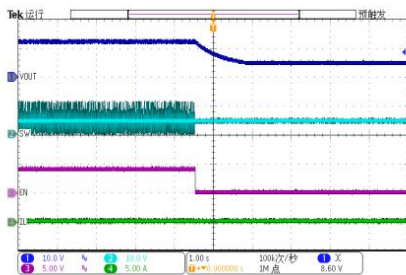
Enable Startup at No Load

$V_{IN} = 5V$, $V_{OUT} = 12V$



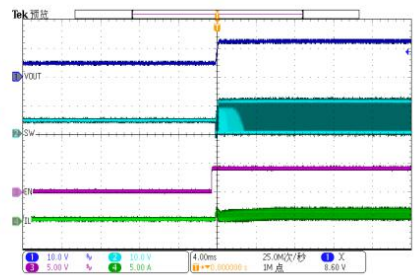
Enable Shutdown at No Load

$V_{IN} = 5V$, $V_{OUT} = 12V$



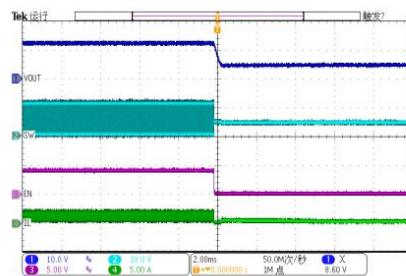
Enable Startup at Heavy Load

$V_{IN} = 5V$, $V_{OUT} = 12V$, $I_{OUT} = 400mA$



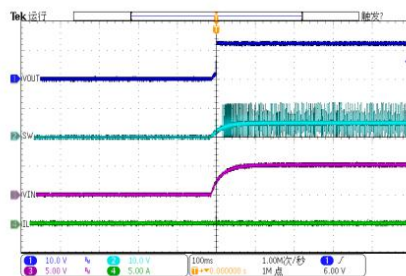
Enable Shutdown at Heavy Load

$V_{IN} = 5V$, $V_{OUT} = 3.3V$, $I_{OUT} = 400mA$



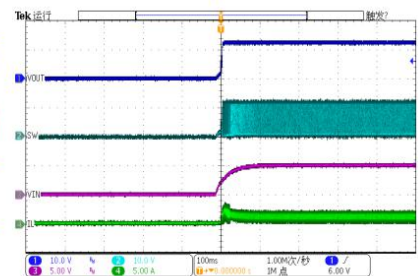
Power Up at No Load

$V_{IN} = 5V$, $V_{OUT} = 12V$, $I_{OUT} = 0A$



Power Up at Heavy Load

$V_{IN} = 5V$, $V_{OUT} = 12V$, $I_{OUT} = 400mA$



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Operation

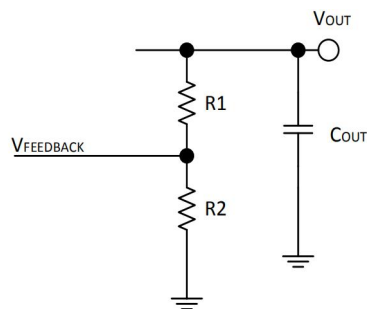
The TX9715 uses a fixed frequency, peak current mode boost regulator architecture to regulate voltage at the feedback pin. The operation of the TX9715 can be understood by referring to the block diagram above. At the start of each oscillator cycle the MOSFET is turned on through the control circuitry. To prevent sub-harmonic oscillations at duty cycles greater than 50 percent, a stabilizing ramp is added to the output of the current sense amplifier and the result is fed into the negative input of the PWM comparator. When this voltage equals the output voltage of the error amplifier the power MOSFET is turned off. The voltage at the output of the error amplifier is an amplified version of the difference between the 0.6V band gap reference voltage and the feedback voltage. In this way the peak current level keeps the output in regulation. If the feedback voltage starts to drop, the output of the error amplifier increases. These results in more current to flow through the power MOSFET, thus increasing the power delivered to the output. The TX9715 has internal soft start to limit the amount of input current at startup and to also limit the amount of overshoot on the output.

Applications Information

Setting the Output Voltage

TX9715 are internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider.

$$V_{OUT} = V_{FB} \times \frac{R1 + R2}{R2}$$



Inductor Selection

The TX9715 boost converter can utilize small surface mount and chip inductors due to the fast 800KHz switching frequency. Inductor values between 2.2μH and 10μH are suitable for most applications. Larger values of inductance will allow slightly greater output current capability by reducing the inductor ripple current. Increasing the inductance above 10μH will increase size while providing little improvement in output current capability. The minimum boost inductance value is given by:

$$L > \frac{V_{IN} \times (V_{OUT} + V_{DIODE} - V_{IN})}{F_S \times I_{RIPPLE} \times (V_{OUT} + V_{DIODE})}$$

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Where

- IRIPPLE: Peak-to-Peak inductor current
- VIN: Input voltage
- VOUT: Output voltage
- VDIODE: Output diode Forward Voltage
- FS: Switching frequency, Hertz

The inductor current ripple is typically set for 20% to 40% of the maximum inductor current. High frequency ferrite core inductor materials reduce frequency dependent power losses compared to cheaper powdered iron types, improving efficiency. The inductor should have low DCR (series resistance of the winding) to reduce the I²R power losses, and must not saturate at peak inductor current levels. Molded chokes and some chip inductors usually.

Capacitor Selection

The internal loop compensation of the TX9715 boost converter is designed to be stable with output capacitor values of 10 μ F or greater. Low ESR (equivalent series resistance) capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have extremely low ESR and are available in small footprints. A 10 μ F to 22 μ F output capacitor is enough for most fixed frequency applications. For applications where Burst Mode operation is enabled, a minimum value of 22 μ F is recommended. Larger values may be used to obtain very low output ripple and to improve transient response. X5R and X7R dielectric materials are preferred for their ability to maintain capacitance over wide voltage and temperature ranges. Y5V types should not be used. Case sizes smaller than 0805 are not recommended due to their increased DC bias effect.

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. It follows that ceramic capacitors are also a good choice for input decoupling and should be located as close as possible to the device. A 22 μ F input capacitor connected to inductor is enough for most applications. Larger values maybe used without limitations. For applications where the power source is more than a few inches away, a larger bulk decoupling capacitor is recommended on the input to the boost converter.

Diode Selection

A Schottky diode should be used for the output diode. The forward current rating of the diode should be higher than the load current, and the reverse voltage rating must be higher than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

PC Board Layout Consideration

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

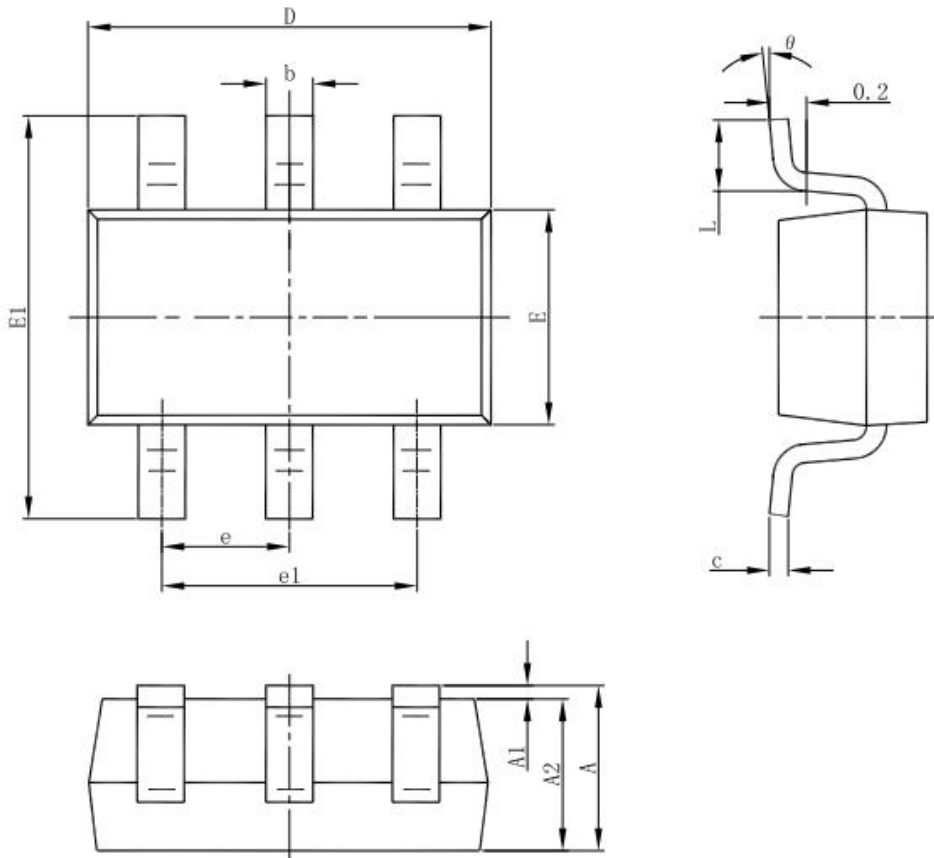
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1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the CIN input capacitor, to the regulator VIN terminal, to the regulator SW terminal, to the inductor then out to the output capacitor COUT and load. The second loop starts from the output capacitor ground, to the regulator GND terminals, to the inductor and then out to COUT and the load. To minimize both loop areas the input capacitor should be placed as close as possible to the VIN terminal. Grounding for both the input and output capacitors should consist of a small localized topside plane that connects to GND. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The SW terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with a enough width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the SW terminals to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the FB terminal. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

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Package Description

6-pin SOT23-6 Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°