500kHz 5A High Efficiency Synchronous PWM Boost Converter

General Description

The FP6276 is a current mode synchronous boost DC-DC converter with PWM/PSM control. Its PWM circuitry with built-in 55mΩ high side switch and 55mΩ low side switch make this regulator highly power efficient. The internal compensation network also minimizes as much as 6 external component counts. The non-inverting input of error amplifier connects to a 0.6V precision reference voltage and internal soft-start function can reduce the inrush current.

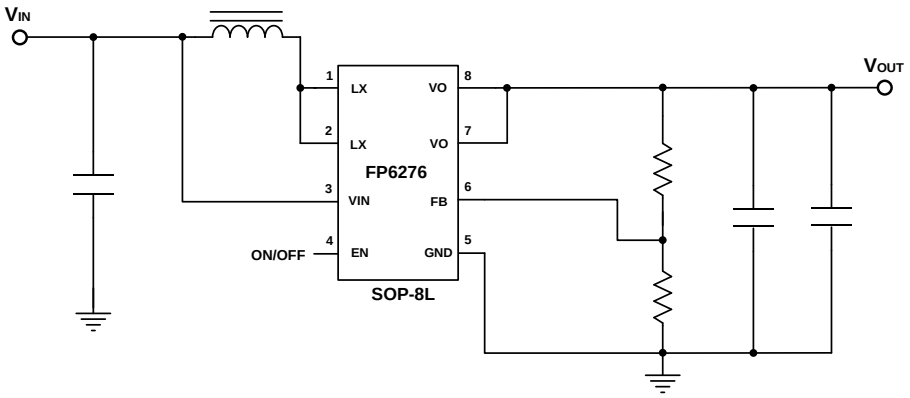
Features

- Current mode with PWM/PSM control
- Input Voltage range: 2.4V~4.5V
- Shutdown current: <1uA
- Oscillator frequency: 500KHz
- Reference voltage: 0.6V +/-2%
- Load disconnect during shutdown
- Cycle-by-cycle current limit
- Low R_{DS}(on): Low side 55mΩ, High side55mΩ.
- Protection: OTP, Output OVP, SCP
- Internal Compensation
- Internal Soft-start: 7ms
- Package: SOP8(EP)

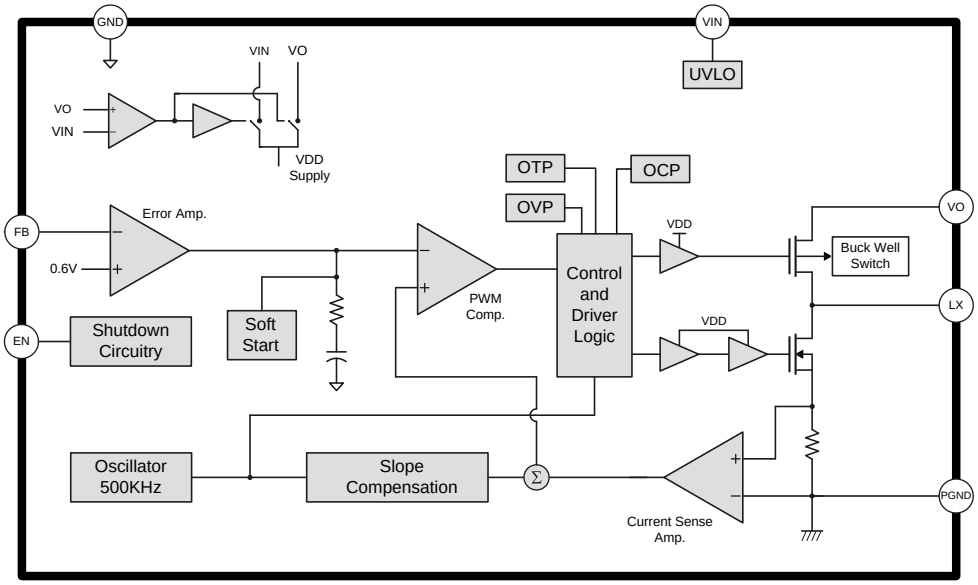
Applications

- Chargers
- Handheld Devices
- Portable Products
- Power Bank

Typical Application Circuit



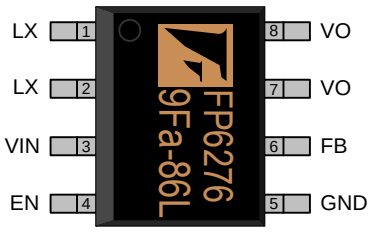
Function Block Diagram



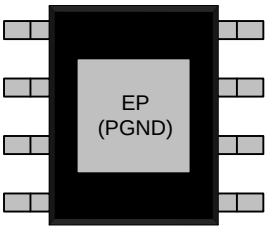
Pin Descriptions

SOP-8L (EP)

Top View



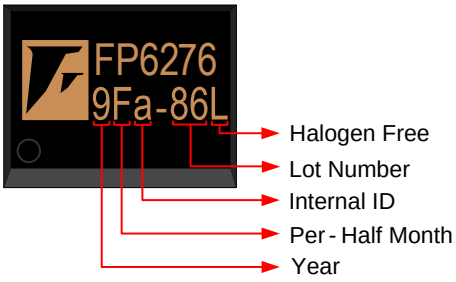
Bottom View



Name	No.	I / O	Description
LX	1	I	Power Switch Output
LX	2	I	Power Switch Output
VIN	3	P	IC Power Supply
EN	4	I	Enable Control (Active High)
GND	5	P	IC Ground
FB	6	I	Error Amplifier Inverting Input
VO	7	O	Output Voltage Pin
VO	8	O	Output Voltage Pin
EP	9	P	IC Power Ground

Marking Information

SOP-8L(EP)



Halogen Free: Halogen free product indicator.

Lot Number: Wafer lot number's last two digits.

For Example: 132386TB → 86

Internal ID: Internal Identification Code.

Per-Half Month: Production period indicated in half month time unit.

For Example: January→A(Front Half Month),B(Last Half Month)

February→C(Front Half Month),D(Last Half Month)

Year: Production year's last digit

Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP6276XR-G1	-40°C ~ 85°C	SOP-8L(EP)	2500EA	Tape & Reel

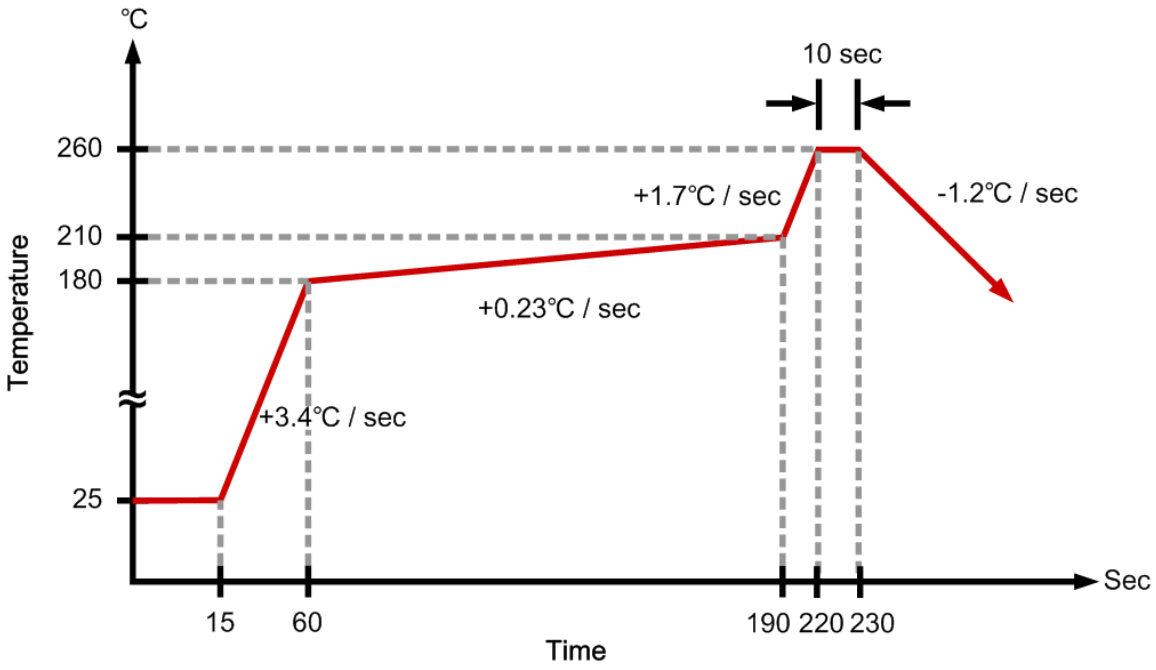
Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{IN}		0		6	V
LX Voltage	V_{LX}		0		6	V
EN,FB Voltage			0		6	V
Thermal Resistance (Note1)	θ_{JA}	SOP-8L(EP)			+83	°C / W
Junction Temperature	T_J				+150	°C
Operating Temperature	T_{OP}		-40		+85	°C
Storage Temperature	T_{ST}		-65		+150	°C
Lead Temperature		(soldering, 10 sec)			+260	°C

Note1:

θ_{JA} is measured in the natural convection at T_A=25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

IR Re-flow Soldering Curve



Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{IN}		2.6		4.5	V
Operating Temperature Range	T_A	Ambient Temperature	-40		+85	°C

DC Electrical Characteristics (V_{IN}=3.3V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Voltage	V_{IN}		2.4		4.5	V
Under Voltage Lockout	V_{UVLO}			2.1		V
UVLO Hysteresis				0.1		V
Quiescent Current	I_{CC}	FB=1.0V, No switch		280		μA
Shutdown Current	I_{CC}	V_{EN}=GND		0.1		μA
Operation Frequency	f_{OSC}	V_{FB}=0.6V		500		kH_Z
Maximum Duty Ratio	%			90		%
Feedback Voltage	V_{REF}	V_{IN}=5V	0.588	0.6	0.612	V
Enable Voltage	V_{EN}		0.96			V
Shutdown Voltage	V_{EN}				0.6	V
Soft-Start Time	t_{SS}	V_{IN}=5V		7		ms
High Side Switch RDS(ON)	$I_{LX(PMOS)}$			55		mΩ
Low Side Switch RDS(ON)	$I_{LX(NMOS)}$			55		mΩ
Switch Current Limit	I_{OCP}			6		A
OVP Threshold Voltage on OUT Pin	V_{OVP}			6		V
Thermal Shutdown Threshold	T_{OTP}			150		℃
Thermal Shutdown Hysteresis				30		℃

Function Description

Operation

The FP6276 is a current mode synchronous boost converter. The constant switching frequency is 500kHz and operates with pulse width modulation (PWM). Build-in 50mΩ high side switch and 50mΩ low side switch provides a high efficient conversion.

Soft Start Function

Soft start circuitry is integrated into FP6276 to avoid inrush current during power on. After the IC is enabled, the output of error amplifier is clamped by the internal soft-start function, which causes PWM pulse width increasing slowly and thus reducing input surge current.

Over Temperature Protection (OTP)

FP6276 will turn off the power MOSFET automatically when the internal junction temperature is over 150°C. The power MOSFET wake up when the junction temperature drops 30°C under the OTP threshold temperature.

Over Voltage Protection (OVP)

In some condition, the resistive divider may be unconnected, which will cause PWM signal to operate with maximum duty cycle and output voltage is boosted higher and higher. The power MOSFET will be turned off immediately, when the output voltage exceeds the OVP threshold level. The FP6276 VO Pin OVP threshold is 6V.

Application Information

Inductor Selection

Inductance value is decided based on different condition. 3.3uH to 4.7μH inductor value is recommended for general application circuit. There are three important inductor specifications, DC resistance, saturation current and core loss. Low DC resistance has better power efficiency. Also, it avoid inductor saturation which will cause circuit system unstable and lower core loss at 500KHz.

Capacitor Selection

The output capacitor is required to maintain the DC voltage. Low ESR capacitors are preferred to reduce the output voltage ripple. Ceramic capacitor of X5R and X7R are recommended, which have low equivalent series resistance (ESR) and wider operation temperature range.

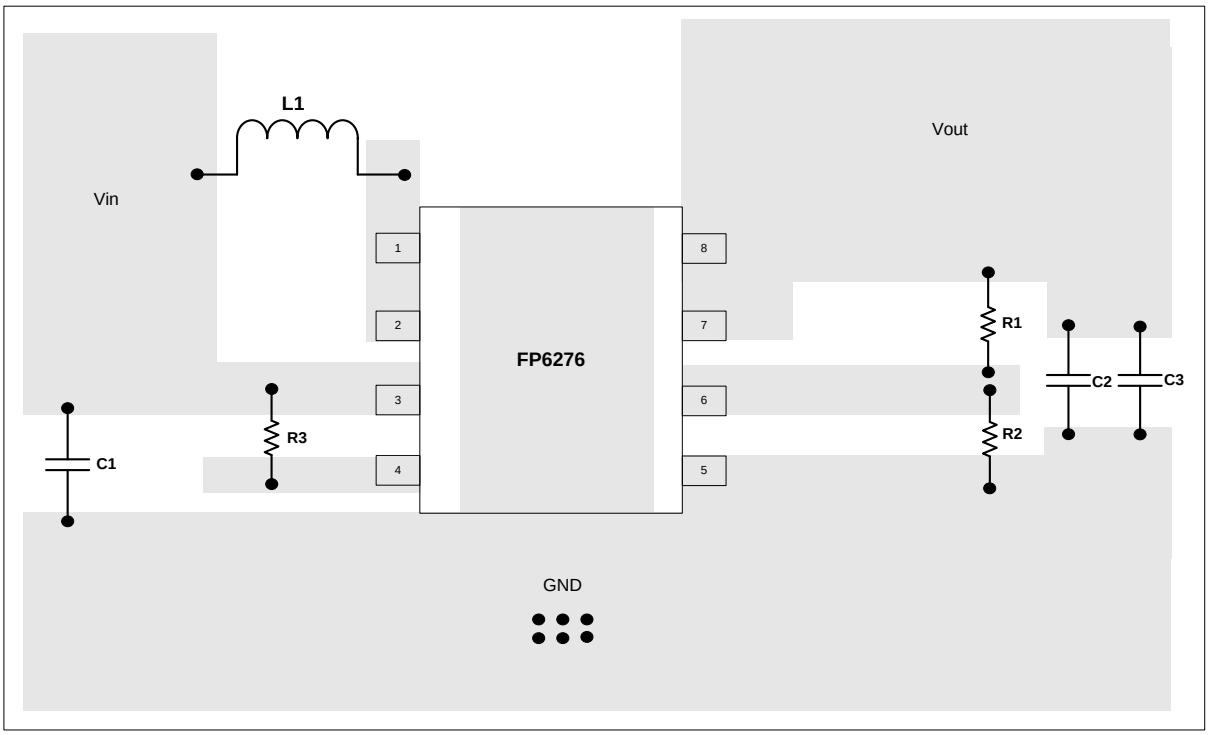
Output Voltage Programming

The output voltage is set by a resistive voltage divider from the output voltage to FB. The output voltage is:

$$V_{OUT} = 0.6V\left(1+\frac{R1}{R2}\right)$$

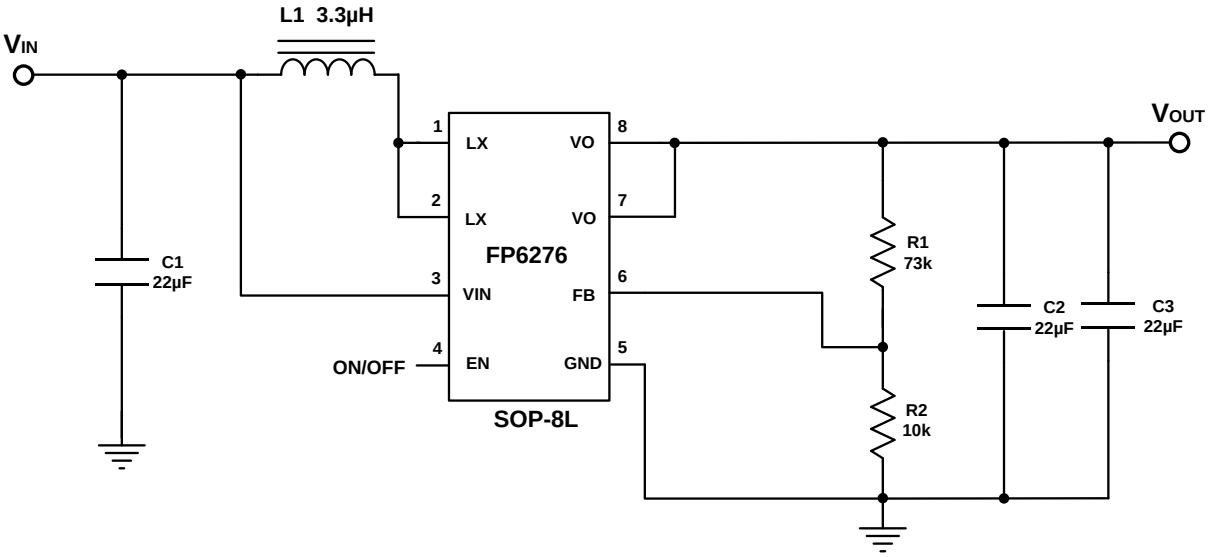
Layout Considerations

1. The power traces, consisting of the GND trace, the LX trace and the V_{IN} trace should be kept short, direct and wide.
2. LX and L switching node, wide and short trace to reduce EMI.
3. Place C_{IN} near V_{IN} pin as closely as possible to maintain input voltage steady and filter out the pulsing input current.
4. The resistive divider R1and R2 must be connected to FB pin directly as closely as possible.
5. FB is a sensitive node. Please keep it away from switching node, LX.
6. The GND of the IC, C_{IN} and C_{OUT} should be connected close together directly to a ground plane.



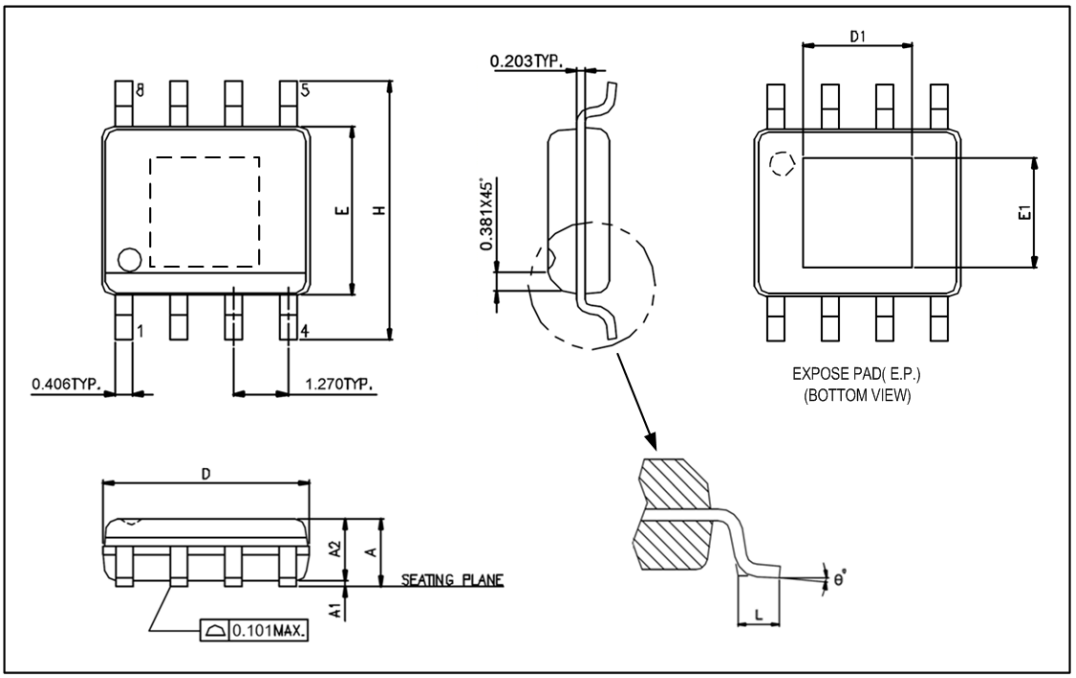
Suggested Layout

Typical Application



Package Outline

SOP-8L (EP)



Unit: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.050	0.152
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Exposed PAD Dimensions:

Symbols	Min. (mm)	Max. (mm)
E1	2.184 REF	
D1	2.971 REF	

Note:

1. Package dimensions are in compliance with JEDEC outline: MS-012 AA.
2. Dimension ”D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E” does not include inter-lead flash or protrusions.