High Efficiency, 1A, Multi-Cell Boost Li-Ion Battery Charger

Check for Samples: JZ5518

特性

- 3.0V to 5.5V Operating Input Voltage
- Up to 26V Sustainable Voltage
- Up to 1A Configurable Charge Current for Battery with 2~4 Cells in Series
- Configurable Input Voltage Limit
- Charge Status Indication
- Constant Voltage Selectable
- Programmable Charge Timeout
- Thermal Regulation Protection
- External Shutdown Function
- Input Voltage UVLO and OVP
- Over Temperature Protection
- Output Short Circuit Protection Normal Synchronous Boost Operation When Battery Removed

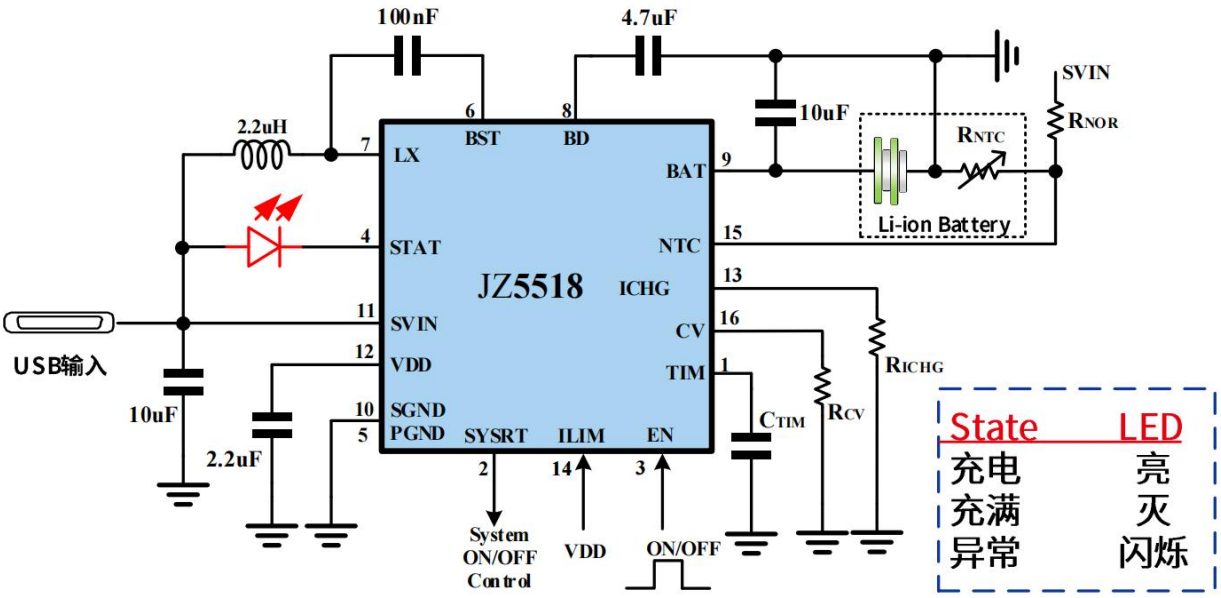
应用

- Power Bank
- Cellular Telephones,MP3Players,MP4 Players
- PSP Game Players,NDS game Players
- Notebook

描述

JZ5518 is a highly integrated synchronous boost charger IC for Lithium-ion batteries with four cells in series. The charge current up to 1A can be programmed by using the external resistor for different portable applications.

Robust protections include input over-voltage protection (OVP), battery OVP, battery short protection, thermal shut down, battery temperature monitor, a configurable timer to prevent prolonged charging of a dead battery.



典型应用拓扑

绝对最大值 (†)

参数	范围
引脚至 GND 电压（SVIN）	-0.3V~20V
引脚至 GND 电压（BAT,BD,LX）	-0.3V~26V
引脚至 GND 电压（ICHG,CV,ILIM ,TIM,SYSRT,NTC,VDD）	-0.3V~5.5V
引脚到 LX 电压（BST）	-0.3V~5.5V
引脚最大电流（LX）	4A
储存温度	-65℃ to 150℃
工作温度	-40℃ to 125℃
ESD 额定值（HBM）	±2KV
ESD 额定值（CDM）	±500V

† 注： 如果器件工作条件超过上述“绝对最大值”，可能引起器件永久性损坏。这仅是极限参数，不建议器件在极限值或超过上述极限值的条件下工作。器件长时间工作在极限条件下可能会影响其可靠性。

引脚排列

表 3.1

ESD(静电放电）敏感器件。
带电器件和电路板可能会在没有察觉的情况下放电。尽管本产品具有专利或专有保护电路，但在遇到高能量 ESD 时，器件可能会损坏。因此，应当采取适当的 ESD 防范措施，以免器件性能下降或者功能丧失。

图 3. 引脚排列（TopView）

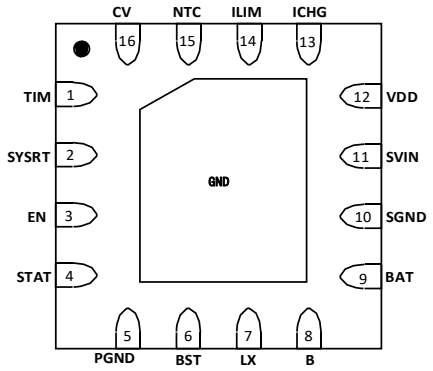


表 3 引脚功能描述

引脚编号	引脚名称	说明
1	TIM	Charge time limit pin. Connect this pin with a capacitor to ground. Internal current source charge and discharges the capacitor for charge time limit. TC charge time limit is about 1/10 of CC charge time.
2	SYSRT	System ON/OFF control pin. When VBAT is lower than 6V, SYSRT pin outputs low logic to turn off the system operation; when VBAT is high than 6V, SYSRT pin outputs high logic to turn on the system operation.
3	EN	Enable control pin. High logic for enable on, and low logic for enable off.
4	STAT	Charge status indication pin. It is open drain output pin and pull high to SVIN thru a LED to indicate the charge in process. When the charge is done, LED is off.
5	PGND	Power ground pin.
6	BST	Boost-Strap pin. Supply Rectified FET’s gate driver. Decouple this pin to LX with 0.1uF ceramic cap.
7	LX	Switch node pin. Connect to external inductor.
8	BD	Connect to the Drain of internal Blocking FET. Bypass a 10uF ceramic cap to GND.
9	BAT	Battery positive pin.

10	SGND	Signal ground pin.
11	SVIN	Analog power input pin. Connect a MLCC from this pin to ground to decouple high harmonic noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage area.
12	VDD	Internal LDO output pin. Bypass at least 2.2uF ceramic cap to GND.
13	ICHG	Charge current program pin, pull down to GND with a resistor RICHG. The mirror current about 1/1000 of the blocking FET current will dump into the external resistor thru ICHG pin and compared to the internal reverence 1V. So ICC (1V/ RICHG)x1000, ITC=(1V/RICHG)x100.
14	ILIM	Adaptive input current limit setting Pin. Connect a resistor divider from SVIN to AGND to configure the minimum input voltage limit threshold.
15	NTC	Thermal protection pin. UTP threshold is typical 75%VSVIN and OTP threshold is typical 25% VSVIN. Pull up to SVIN can disable charge logic and make the IC operate as normal boost regulator.
16	CV	Battery CV voltage selection pin.
EP	GND	封装底部焊盘，连接到 GND，并连接到一个大的平面，达到较好的散热。

（1） DI = input, O = output, P = power.

功能框图

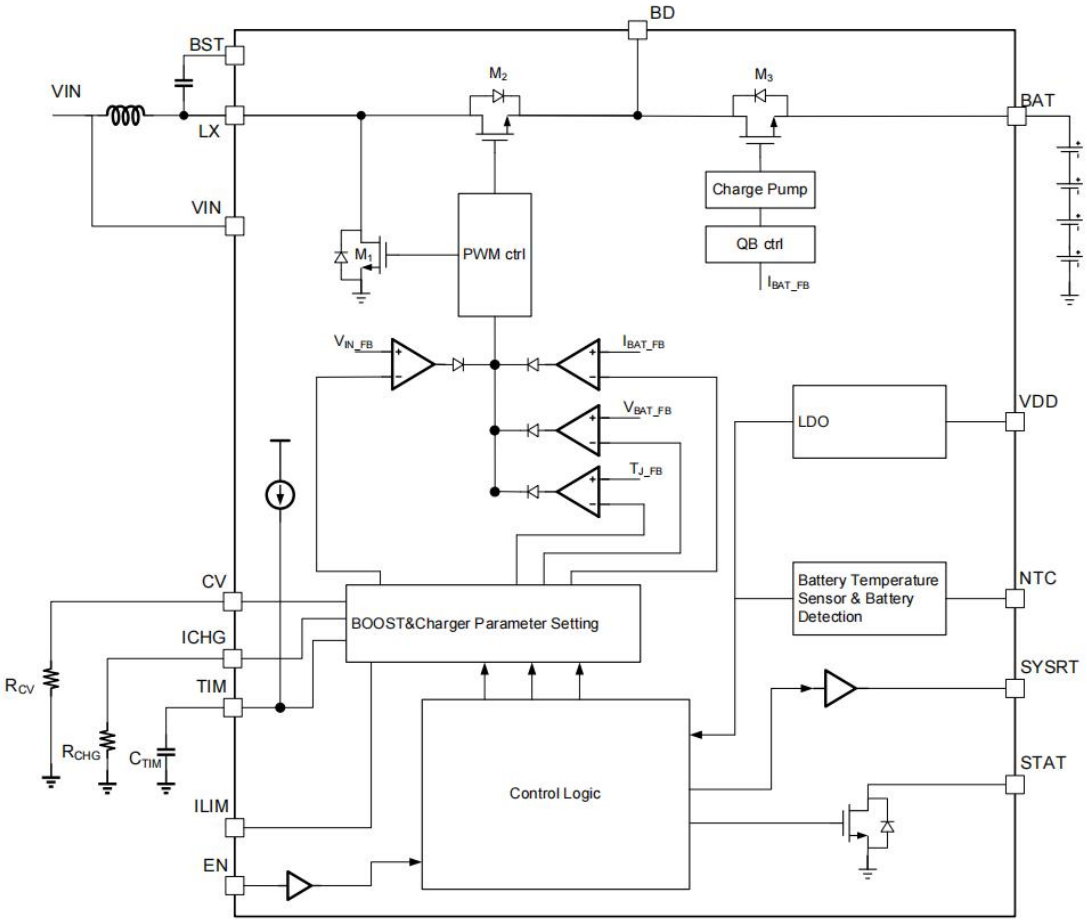


图 4. 内部功能框图

技术规格

除非有特殊说明，否则极限值适用于-40℃至+125℃的工作结温度（TJ）范围。最小和最大限值通过试验，验证和统计相关性规定。典型值代表 TJ=25℃时最可能的参数规范，仅供参考。所有电压都是相对于 GND。

表 5.

参数		测试条件	最小值	典型值	最大值	单位
Bias Supply (V_{SVIN})						
V_{SVIN}	Supply voltage		3	5	5.5	V
V_{UVLO}	V_{SVIN} under voltage lockout threshold	V_{SVIN} rising and measured			2.9	V
ΔV_{UVLO}	V_{SVIN} under voltage lockout	Measured from V_{SVIN} to GND		100		mV
V_{OVP}	Input overvoltage protection	V_{SVIN} rising and measured		6		V
Quiescent Current						
I_{BAT}	Battery discharge current	Shutdown IC			25	μA
I_{IN}	Input quiescent current	Disable Charge			1.5	mA
Oscillator and PWM(TBD)						
f_{SW}	Switching frequency			1000		kHz
T_{MINOFF}	Main N-FET minimum off time	With 16V rating				ns
T_{MAXOFF}	Main N-FET maximum off time	With 16V rating				μs
T_{MINON}	Main N-FET minimum on time	With 16V rating				ns
Power MOSFET						
R_{NFET_M}	$R_{DS(ON)}$ of Main N-FET			100		mΩ
R_{NFET_R}	$R_{DS(ON)}$ of Rectified N-FET			80		mΩ
R_{NFET_B}	$R_{DS(ON)}$ of Blocking N-FET			60		mΩ
Voltage Regulation						
V_{CV}	2-Cell battery charge voltage configuration	R_{CV}= 2.5k	8.32	8.4	8.48	V
		R_{CV}= 7.5k	8.51	8.6	8.69	V
		R_{CV}= 25k	8.61	8.7	8.79	V
		R_{CV}= 75k	8.71	8.8	8.89	V
	3-Cell battery charge voltage configuration	R_{CV}= 2.5k	12.47	12.6	12.73	V
		R_{CV}= 7.5k	12.77	12.9	13.03	V
		R_{CV}= 25k	12.92	13.05	13.18	V
		R_{CV}= 75k	13.07	13.2	13.33	V
	4-Cell battery charge voltage configuration	R_{CV}= 2.5k	16.63	16.8	16.97	V
		R_{CV}= 7.5k	17.03	17.2	17.37	V
		R_{CV}= 25k	17.23	17.4	17.57	V
		R_{CV}= 75k	17.42	17.6	17.78	V
ΔV_{RCH}	2-Cell Recharge Voltage		100	200	300	mV
	3-Cell Recharge Voltage			300		mV
	4-Cell Recharge Voltage			400		mV
V_{TRK}	2-cell TC charge mode battery voltage threshold	R_{CV}=10k, V_{BAT} rising edge threshold	-2%	5.6	+2%	V
	3-cell TC charge mode battery voltage threshold	R_{CV}=10k, V_{BAT} rising edge threshold	-2%	8.4	+2%	V
	4-cell TC charge mode battery voltage threshold	R_{CV}=10k, V_{BAT} rising edge threshold	-2%	11.2	+2%	V
Battery Connect Detection						
V_{DET}	NTC voltage threshold for Battery detect	NTC Falling Edge	85%		95%	VDD

Charge Current						
I_{CC}	Internal charge current accuracy for Constant Current Mode	I_{CC}=1000mA	-10%		10%	
	Internal charge current accuracy for Trickle Current Mode	I_{TC}=100mA	-50%		50%	
I_{TERM}	Termination current	I_{CC}=1000mA	50	100	150	mA
Output Voltage OVP						
V_{OVP}	Output voltage OVP threshold			105%		VCV
Timer						
T_{TC}	Trickle current charge timeout	C_{TIM}=330nF	0.425	0.5	0.575	hour
T_{CC}	Constant current charge timeout		3.825	4.0	5.175	hour
T_{MC}	Charge mode change delay time			30		ms
T_{TERM}	Termination delay time			30		ms
T_{RCHG}	Recharge time delay			30		ms
Short Circuit Protection						
V_{SHORT}	Output short protection threshold		1.7	2	2.3	V
System ON/OFF Control						
V_{HSYSRT}	High logic of system ON/OFF control	I(OH)=-1mA，VIN=5V	VDD -0.8	VDD -0.9	VDD +1.1	V
V_{LSYSRT}	Low logic of system ON/OFF control	I(OL)= 1mA，VIN=5V	0.7	0.9	1	V
Linear charger Mode						
I_{LCHG}	Battery Charger current when the blocking FET is in linear mode	V_{BAT}<V_{SHORT}		5%		I_{CC}
I_{LPEAK}	Peak linear current when Battery is absent			1		A
V_{BD}	Bus voltage regulation		5.8	6	6.2	V
				9		V
				11.6		V
V_{TRON}	Blocking FET fully turn on threshold V_{TRON}=V_{BAT}-V_{IN}	V_{BAT} > V_{TRK}		100		mV
Enable ON/OFF Control						
V_{ENH}	High level logic for enable control		1.5			V
V_{ENL}	Low level logic for enable control				0.4	V
Battery Thermal Protection NTC						
UTP	Under temperature protection		70%	75%	80%	V_{SVIN}
	Under temperature protection Hysteresis	Falling edge		5%		V_{SVIN}
OTP	Over temperature protection		28%	30%	32%	V_{SVIN}
	Over temperature protection hysteresis	Rising edge		2%		V_{SVIN}
Thermal Regulation and Thermal shutdown						
T_{REG}	Thermal regulation threshold			120		°C
T_{REGHYS}	Thermal regulation hysteresis falling edge			20		°C
TSD	Thermal shutdown temperature	Rising Threshold		160		°C
TSD_{HYS}	Thermal shutdown temperature hysteresis			30		°C

应用信息： Multi-Cell Boost Li-Ion Battery Charger

概述

JZ5518 是一款升压型 2~4 节锂电池充电管理器。

正常充电循环

The JZ5518 provides four main charging phases: short mode, pre-charge, constant current charge mode, constant voltage charge mode.

Short mode: When VBAT is lower than VSHORT (typically 2V), the Boost works in light load, blocking FET works in linear mode, and the battery will be charged through body diode of HS FET by 5% ICC.

Pre-charge mode: When VBAT exceeds pre-charge voltage VSHORT, the Boost works in light load and regulates the VBD and 6V and blocking FET works in linear mode. The charge current is 20% of ICC. If duration of pre-charge exceeds 0.5 hour, VBAT is lower than the threshold of trickle voltage VTRK (typically 8.4V), the charge mode turns off, abnormal status is indicated through STAT.

Constant current mode: When VBAT is higher than the threshold of VTRK, the blocking FET fully turns on, the Boost works in constant current mode, and the charge current is ICC.

Constant voltage mode: When VBAT reaches regulation voltage, the charge current begins to decrease. The charge cycle is complete once the constant voltage loop is domain.

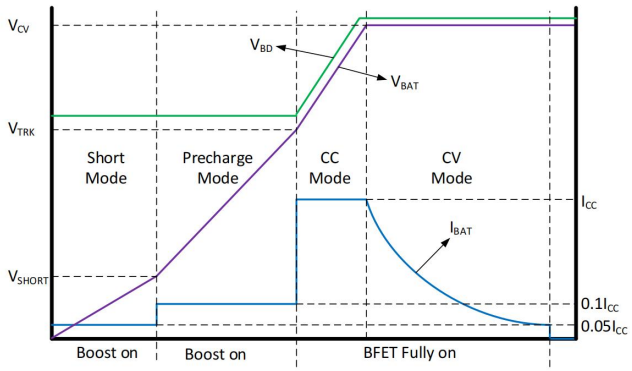


图 7.电池充电循环

充电挡位选择

The JZ5518 has a CV pin that can configure the battery regulation voltage. When CV is connected to AGND via a resistor, the battery regulation voltage is set by the resistance according to Table.

Resistor Range V_{BATT_REG}	Resistor Range V_{BATT_REG}
2.5k	8.4V
7.5k	8.6V
25k	8.7V
75k	8.8V

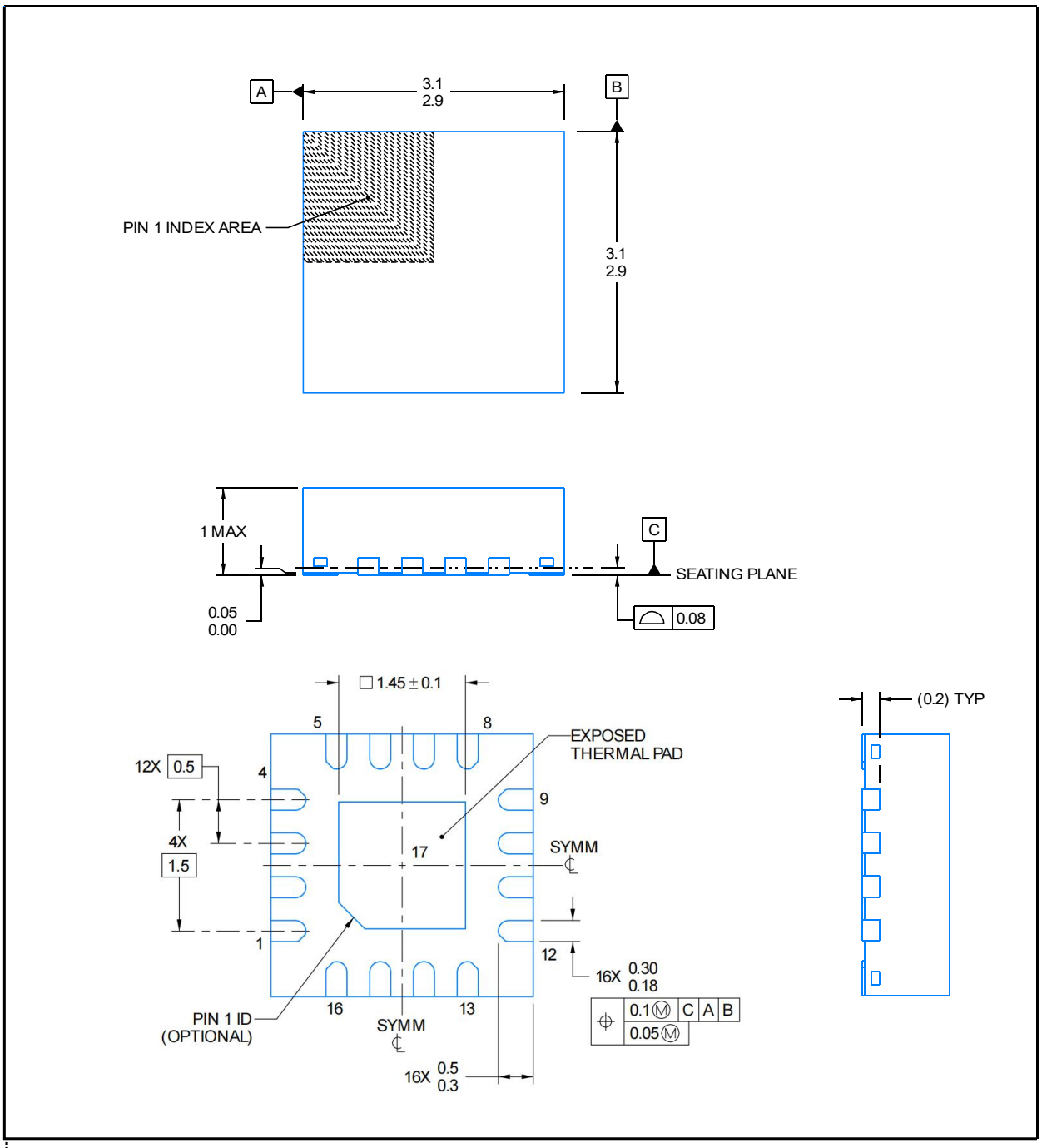
电池检测

The JZ5518 is capable of detect whether a battery is connected. When the voltage of NTC is higher than 85%~95% of VIN, the battery missing flag BAT_MISS_STAT bit is set 1.

If BAT_MISS_STAT is high, JZ5518 works in switching mode boost converter. When VIN is higher than UVLO threshold, the blocking FET is softly turned on. After blocking FET fully turns on, switching mode boost converter starts work.

封装外形描述(QFN16)

具备底部 PAD 的 16 引脚塑封 SOIC



注：

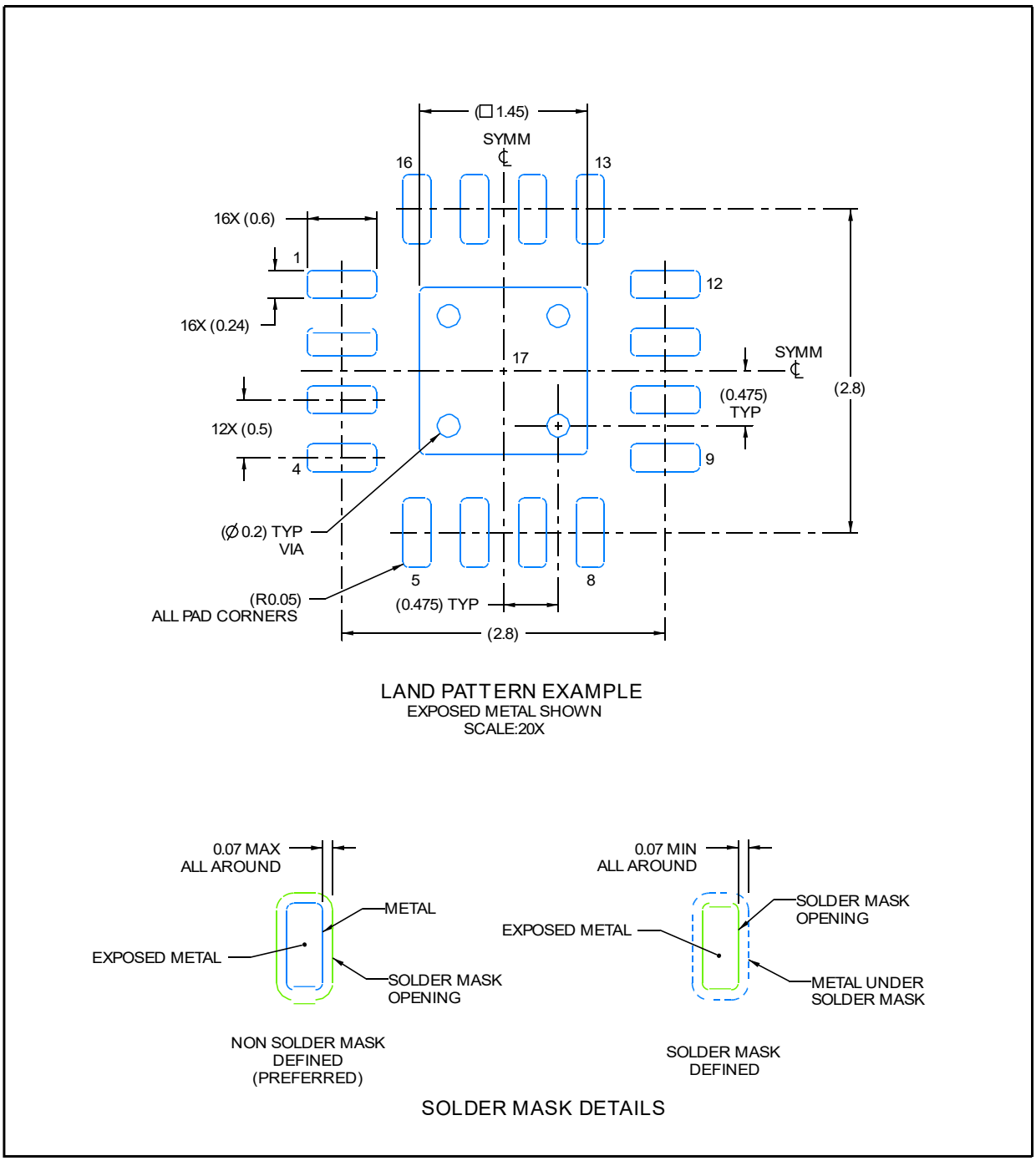
（1）所有的数据单位都是毫米，括号内的任何尺寸仅供参考。尺寸和公差符合 ASME Y14.5M.

（2）本图如有更改，恕不另行通知。

（3）此尺寸不包括塑模毛边，突起，或水口毛刺。塑模每侧的毛边或突起不超过 0.15 毫米。

（4）此尺寸不包括塑模毛边，塑模每侧的毛边或突起不超过 0.25 毫米。

器件封装焊盘布局举例(QFN16)



注：

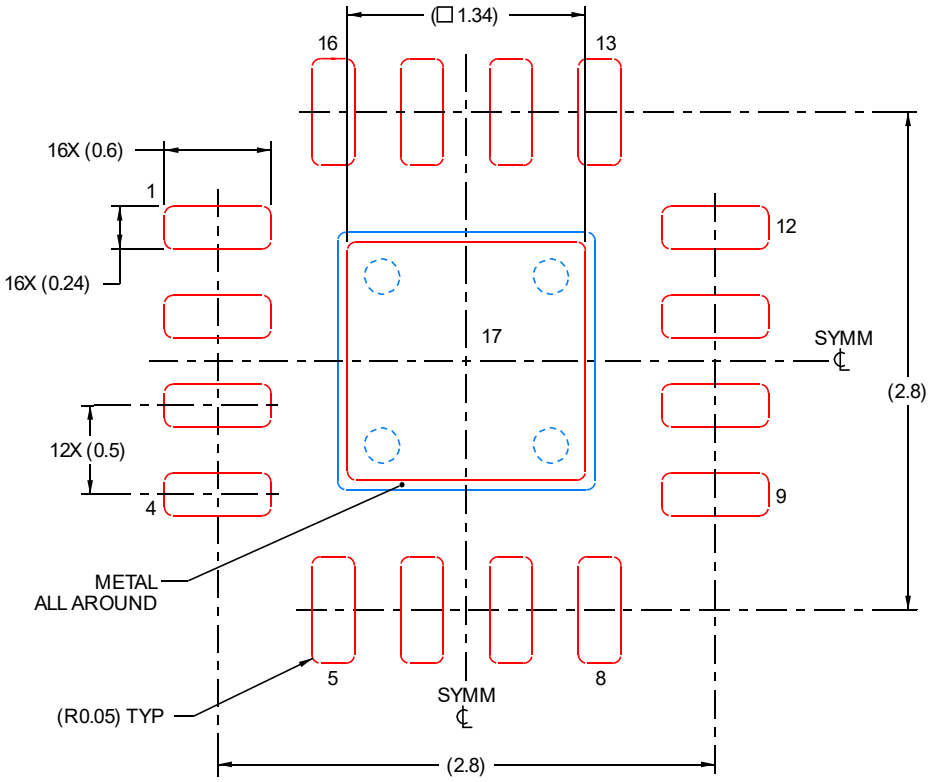
（1）基于 IPC-7351 依赖于久经考验的数学算法，综合考虑了制造、组装和元件容差，从而精确计算的焊盘图形 。

（2）信号焊盘之间和周围的焊接掩膜公差可能因电路板制造而异。

（3）金属垫的尺寸可能因爬电要求而异。

（4）通孔是可选的，取决于应用，请参阅器件数据表。如果使用了过孔，请参考此视图中所示的过孔位置。建议 填充、或用锡膏盖住焊盘下的过孔。

器件封装焊盘布局举例(continued)



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

注：

（5）基于 IPC-7351 依赖于久经考验的数学算法，综合考虑了制造、组装和元件容差，从而精确计算的焊盘图形 。

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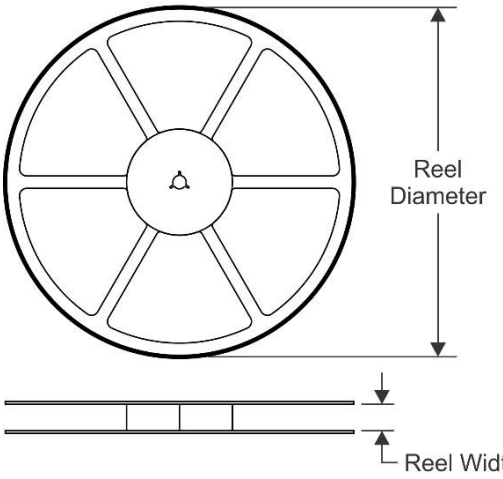
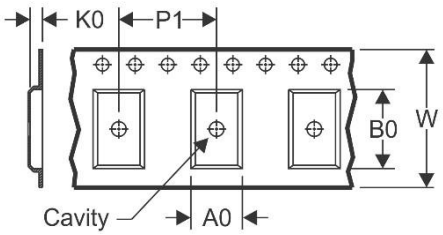
TAPE AND REEL INFORMALEGEND-SION

REEL DIMENSIONS

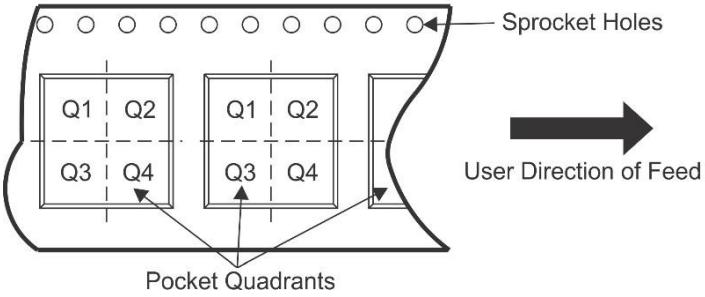


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*ALL dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
JZ5518	DFN16	D										

TAPE AND REEL BOX DIMENSIONS